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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
SP088.C6APPLICATION NO.
10/083,143APPLICANT
Deosaran *et al.*FILING DATE
February 27, 2002GROUP
2172 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
WMT	AA1	4,626,989	12/1986	Torii	364	200	
	AB1	4,675,806	06/1987	Uchida	364	200	
	AC1	4,722,049	01/1988	Lahti	364	200	
	AD1	4,807,115	02/1989	Tornig	364	200	
	AE1	4,901,233	02/1990	Liptay	364	200	
	AF1	4,903,196	02/1990	Pomeroy	364	200	
	AG1	4,942,525	07/1990	Shintani <i>et al.</i>	364	200	
	AH1	4,992,938	02/1991	Cocke <i>et al.</i>	364	200	
WMT	AI1	5,067,069	11/1991	Fite <i>et al.</i>	395	375	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
WMT	AJ1	WO 88/09035 A2	11/1988	PCT	G11C	8/00	N/A
	AK1	WO 91/20031 A1	12/1991	PCT	G06F	9/45	N/A
	AL1	0 378 195 A2 & A3	07/1990	EP	G06F	5/06	N/A
WMT	AM1	0 515 166 A1	11/1992	EP	G06F	9/38	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	1	Acosta, R. D. <i>et al.</i> , "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," <i>IEEE Transactions On Computers</i> , IEEE, Vol. C-35, No. 9, pp. 815-828 (September 1986).
	AO	1	Agerwala, T. and Cocke, J., "High Performance Reduced Instruction Set Processors," IBM Research Division, pp. 1-61 (March 31, 1987).
	AP	1	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique," <i>Proceedings of the 1988 ESOP</i> , Springer-Verlag, pp. 221-235 (1988).
	AQ	1	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," <i>Computer</i> , IEEE, Vol. 14, pp. 18-27 (September 1981).
WMT	AR	1	Colwell, R.P. <i>et al.</i> , "A VLIW Architecture for a Trace Scheduling Compiler," <i>Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems</i> , ACM, pp. 180-192 (October 1987).

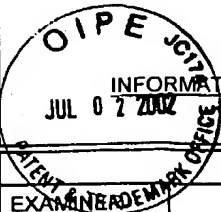
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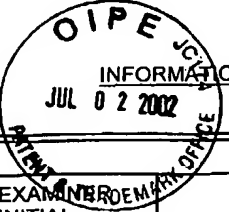
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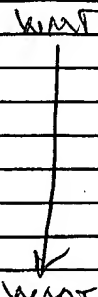
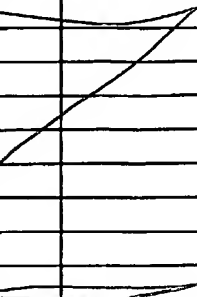
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				APPLICANT Deosaran <i>et al.</i>			
				FILING DATE February 27, 2002		GROUP 2112 2183	
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	AB2	5,109,495	04/1992	Fite <i>et al.</i>	395	375	
	AC2	5,142,633	08/1992	Murray <i>et al.</i>	395	375	
	AD2	5,167,026	11/1992	Murray <i>et al.</i>	395	375	
	AE2	5,214,763	05/1993	Blaner <i>et al.</i>	395	375	
	AF2	5,222,244	06/1993	Carbine <i>et al.</i>	395	800	
	AG2	5,226,126	07/1993	McFarland <i>et al.</i>	395	375	
	AH2	5,230,068	07/1993	Van Dyke <i>et al.</i>	395	375	
AI2	5,251,306	10/1993	Tran	395	375		
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WMT	AN	2	Dwyer, H. A <i>Multiple, Out-of-Order Instruction Issuing System for Superscalar Processors</i> , UMI, pp. 1-249 (August 1991).				
	AO	2	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," <i>IEEE Transactions On Computers</i> , IEEE, pp. 1411-1415 (December 1971).				
	AP	2	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," <i>International Conference on Supercomputing</i> , ACM, pp. 442-452 (1988).				
	AQ	2	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," <i>Proceedings of the 5th Annual Workshop on Microprogramming</i> , IEEE, pp. 114-120 (October 5-7, 1982).				
	AR	2	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," <i>Proceedings 1989 IEEE International Conference on Computer Design: VLSI in Computers and Processors</i> , IEEE, pp. 134-137 (October 1989).				
EXAMINER W. TREAT				DATE CONSIDERED 9/17/04			

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				FILING DATE February 27, 2002		GROUP 2172 <u>2163</u>	

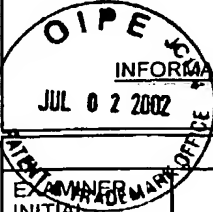
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	AA3	5,255,384	10/1993	Sachs <i>et al.</i>	395	425	
	AB3	5,261,071	11/1993	Lyon	395	425	
	AC3	5,278,963	01/1994	Hattersley <i>et al.</i>	395	400	
	AD3	5,317,720	05/1994	Stamm <i>et al.</i>	395	425	
	AE3	5,345,569	09/1994	Tran	395	375	
	AF3	5,355,457	10/1994	Shebanow <i>et al.</i>	395	375	
	AG3	5,371,684	12/1994	Iadonato <i>et al.</i>	395	491	
	AH3	5,398,330	03/1995	Johnson	395	575	
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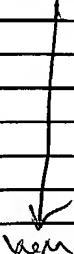
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
	AN	3	Horst, R.W. <i>et al.</i> , "Multiple Instruction Issue in the NonStop Cyclone Processor," <i>Proceedings of the 17th Annual International Symposium on Computer Architecture</i> , IEEE, pp. 216-226 (1990).
	AO	3	Hwu, W-M. W. and Patt, Y.N., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," <i>IEEE Trans. On Computers</i> , IEEE, Vol. C-36, No. 12, pp. 1496-1514 (December 1987).
	AP	3	Hwu, W-M. W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," <i>Proceedings of the 15th Annual Symposium on Computer Architecture</i> , IEEE, pp. 45-53 (June 1988).
	AQ	3	Hwu, W-M. and Patt, Y.N., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," <i>Proceedings from ISCA-13</i> , IEEE, pp. 297-306 (June 2-5, 1986).
	AR	3	IBM <i>Journal of Research and Development</i> , IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).


EXAMINER <u>W. TREAT</u>	DATE CONSIDERED <u>9/17/04</u>
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				FILING DATE February 27, 2002		GROUP 2472 2183	


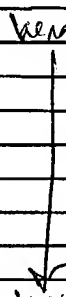
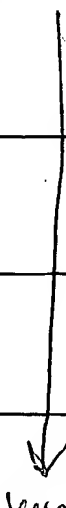
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	AA4	5,448,705	09/1995	Nguyen <i>et al.</i>	395	375	
	AB4	5,487,156	01/1996	Popescu <i>et al.</i>	395	375	
	AC4	5,497,499	03/1996	Garg <i>et al.</i>	395	800	
	AD4	5,524,225	06/1996	Kranich	395	403	
	AE4	5,560,032	09/1996	Nguyen <i>et al.</i>	395	800	
	AF4	5,561,776	10/1996	Popescu <i>et al.</i>	395	375	
	AG4	5,574,927	11/1996	Scantlin	395	800	
	AH4	5,590,295	12/1996	Deosaran <i>et al.</i>	395	393	
	AI4	5,592,636	01/1997	Popescu <i>et al.</i>	395	586	

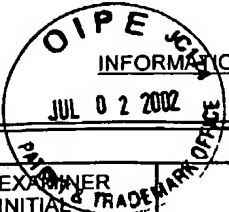
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4						
	AK4						
	AL4						
	AM4						


OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
	AN	4	Johnson, M. <i>Superscalar Microprocessor Design</i> , Prentice-Hall, Entire book submitted (1991).
	AO	4	Johnson, W. M., <i>Super-Scalar Processor Design</i> , (Dissertation), 134 pages (1989).
	AP	4	Jouppi, N.P. and Wall, D.W., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," <i>Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems</i> , ACM, pp. 272-282 (April 1989).
	AQ	4	Jouppi, N.P., "Integration and Packaging Plateaus of Processor Performance," <i>International Conference of Computer Design</i> , IEEE, pp. 229-232 (October 1989).
	AR	4	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," <i>IEEE Transactions on Computers</i> , IEEE, Vol. 38, No. 12, pp. 1645-1658 (December 1989).

EXAMINER W. TREAT		DATE CONSIDERED 9/17/04
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE	
	AA5	5,606,676	02/1997	Grochowski <i>et al.</i>	995	586	
	AB5	5,619,668	04/1997	Zaidi	395	376	
	AC5	5,625,837	04/1997	Popescu <i>et al.</i>	395	800	
	AD5	5,627,983	05/1997	Popescu <i>et al.</i>	395	393	
	AE5	5,708,841	01/1998	Popescu <i>et al.</i>	395	800	
	AF5	5,737,624	04/1998	Garg <i>et al.</i>	395	800.23	
	AG5	5,768,575	06/1998	McFarland <i>et al.</i>	395	569	
	AH5	5,778,210	07/1998	Henstrom <i>et al.</i>	395	394	
	AI5	5,797,025	08/1998	Popescu <i>et al.</i>	395	800	
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	AJ5						
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AN	5	Keller, R.M., "Look-Ahead Processors," <i>Computing Surveys</i> , ACM, Vol. 7, No. 4, pp. 177-195 (December 1975).				
	AO	5	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," <i>Annu. Rev. Comput. Sci.</i> , Annual Reviews, Vol. 4, pp. 173-201 (1990).				
	AP	5	Lightner, B.D. and Hill, G., "The Metaflow Lightning Chipset", <i>Compcon Spring 91</i> , IEEE, pp. 13-18 (February 25 - March 1, 1991).				
	AQ	5	Murakami, K. <i>et al.</i> , "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," <i>Proc. 16th Int. Symp. on Computer Architecture</i> , ACM, pp.78-85 (June 1989).				
	AR	5	Patt, Y.N. <i>et al.</i> , "Critical Issues Regarding HPS, A High Performance Microarchitecture", <i>Proceedings of 18th Annual Workshop on Microprogramming</i> , IEEE, pp. 109-116 (December 3-6, 1985).				
EXAMINER W. TREAT				DATE CONSIDERED 9/17/04			
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				FILING DATE February 27, 2002		GROUP 2172 2183	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
WMT	AA6	5,809,276	09/1998	Deosaran <i>et al.</i>	395	393	
	AB6	5,832,205	11/1998	Kelly <i>et al.</i>	395	185.06	
	AC6	5,832,293	11/1998	Popescu <i>et al.</i>	395	800-23	
	AD6	6,138,231	10/2000	Deosaran <i>et al.</i>	712	216	
WMT	AE6	6,272,617 B1	08/2001	Deosaran <i>et al.</i>	712	23	
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WMT	AN	6	Patt, Y.N. <i>et al.</i> , "HPS, A New Microarchitecture: Rationale and Introduction", <i>The 18th Annual Workshop on Microprogramming</i> , Pacific Grove, CA, December 3-6, 1985, IEEE Computer Society Order No. 653, pp. 103-108.				
	AO	6	Patterson, D.A. and Hennessy, J.L., <i>Computer Architecture: A Quantitative Approach</i> , Morgan Kaufmann Publishers, pp. 257-278, 290-314 and 449 (1990).				
	AP	6	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching and their CISC Performance Potential", IEEE, pp. 263-266 (1991).				
	AQ	6	Pleszkun, A.R. and Sohi, G.S., "The Performance Potential of Multiple Functional Unit Processors," <i>Proceedings of the 15th Annual Symposium on Computer Architecture</i> , IEEE, pp. 37-44 (June 1988).				
WMT	AR	6	Pleszkun, A.R. <i>et al.</i> , "WISQ: A Restartable Architecture Using Qu u s," <i>Proceedings of the 14th International Symposium on Computer Architecture</i> , ACM, pp. 290-299 (June 1987).				
EXAMINER WMT TRBAT					DATE CONSIDERED 9/17/04		
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	INFORMATION DISCLOSURE STATEMENT	APPLICANT Deosaran <i>et al.</i>	
		FILING DATE February 27, 2002	GROUP 2472 2163

U.S. PATENT DOCUMENTS

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
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FOREIGN PATENT DOCUMENTS


EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7						
	AK7						
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	Z	Popescu, V. <i>et al.</i> , "The Metaflow Architecture", <i>IEEE Micro</i> , IEEE, Vol. 11, No.3, pp. 10-13 and 63-73 (June 1991).
	AO	Z	Smith, M.D. <i>et al.</i> , "Boosting Beyond Static Scheduling in a Superscalar Processor," <i>International Symposium on Computer Architecture</i> , IEEE, pp. 344-354 (May 1990).
	AP	Z	Smith, J.E. and Pleszkun, A.R., "Implementation of Precise Interrupts in Pipelined Processors," <i>Proceedings of the 12th Annual International Symposium on Computer Architecture</i> , IEEE, pp. 36-44 (June 1985).
	AQ	Z	Smith, M.D. <i>et al.</i> , "Limits on Multiple Instruction Issue," <i>Computer Architecture News</i> , ACM, No. 2, pp. 290-302 (April 3-6, 1989).
	AR	Z	Sohi, G.S. and Vajapeyam, G.S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," <i>Conference Proceedings of the 14th Annual International Symposium on Computer Architecture</i> , pp. 27-34 (June 2-5, 1987).

EXAMINER <i>W. TR EAT</i>	DATE CONSIDERED <i>9/17/04</i>
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	FILING DATE February 27, 2002	GROUP 2172 2183

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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	AM8					

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WENT	AN	8	Thornton, J.E., <i>Design of a Computer: The Control Data 6600</i> , Control Data Corporation, pp. 58-140 (1970).
	AO	8	Tjaden, G.S. and Flynn, M.J., "Detection and Parallel Execution of Independent Instructions," <i>IEEE Trans. On Computers</i> , IEEE, Vol. C-19, No. 10, pp. 889-895 (October 1970).
	AP	8	Tjaden, G.S. and Flynn, M.J. <i>Representation and Detection of Concurrency Using Ordering Matrices</i> , (Dissertation), UMI, pp. 1-199 (1972).
	AQ	8	Tjaden <i>et al.</i> , "Representation of Concurrency with Ordering Matrices," <i>IEEE Transactions On Computers</i> , IEEE, Vol. C-22, No. 8, pp. 752-761 (August 1973).
WENT	AR	8	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," <i>IBM Journal</i> , IBM, Vol. 11, pp. 25-33 (January 1967).

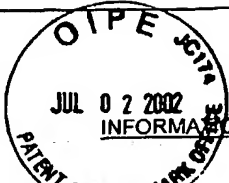
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U.S. PATENT DOCUMENTS


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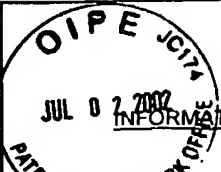
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
		AJ9					
		AK9					
		AL9					
		AM9					

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	9	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," <i>Proceedings of the 19th Annual Hawaii International Conference on System Sciences, HICSS</i> , pp. 41-50 (1986).
	AO	9	Wedig, R.G., <i>Detection of Concurrency In Directly Executed Language Instruction Streams</i> , (Dissertation), UMI, pp. 1-179 (June 1982).
	AP	9	Weiss, S. and Smith, J.E., "Instruction Issue Logic in Pipelined Supercomputers," <i>IEEE Trans. on Computers</i> , IEEE, Vol. C-33, No. 11, pp. 1013-1022 (November 1984).
	AQ	9	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 23, 1990).
	AR	9	Butler, M. and Patt, Y., "An Investigation of the Performance of Various Dynamic Scheduling Techniques," <i>Proceedings from MICRO-25</i> , pp. 1-9 (December 1-4, 1992).

EXAMINER W. TREAT	DATE CONSIDERED 9/17/04
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

	FORM PTO-1449		ATTY. DOCKET NO. SP088.C6	APPLICATION NO. 10/083,143
	INFORMATION DISCLOSURE STATEMENT			
	APPLICANT Deosaran <i>et al.</i>		GROUP 2172, 2183	
	FILING DATE February 27, 2002			

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AJ10					
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	AL10					
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	10	Butler, M. <i>et al.</i> , "Single Instruction Stream Parallelism Is Greater than Two," <i>The 18th Annual International Symposium on Computer Architecture</i> , ACM SIGARCH, Vol. 19, No. 3, pp. 276-286 (May 1991).
	AO	10	Gee, J. <i>et al.</i> , "The Implementation of Prolog via VAX 8600 Microcode," IEEE, pp. 68-74 (1986).
	AP	10	Hwu, W.-M. <i>et al.</i> , "An HPS Implementation of VAX: Initial Design and Analysis," <i>Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences</i> , pp. 282-291 (1986).
	AQ	10	Hwu, W.-M. <i>et al.</i> , "Design Choices for the HPSm Microprocessor Chip," <i>Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences</i> , pp. 330-336 (1987).
WMT	AR	10	Hwu, W.-M. and Patt, Y.N., "HPSm2: A Refined Single-Chip Microengine," <i>HICSS '88</i> , pp. 30-40, 1988.


EXAMINER

W. TREAT

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 FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP088.C6	APPLICATION NO. 10/083,143
	APPLICANT Deosaran <i>et al.</i>	
	FILING DATE February 27, 2002	GROUP 2172 2183

U.S. PATENT DOCUMENTS						
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	AN	11	Kateveris, Hardware Support "Thesis," pg. 138-145 (1984).
	AO	11	Melvin, S. and Patt, Y., "Exploiting Fine-Grained Parallelism Through a Combination of Hardware and Software Techniques," <i>The 18th Annual International Symposium on Computer Architecture, ACM SIGARCH</i> , Vol. 19, No. 3, pp. 287-296 (May 1991).
	AP	11	Patt, Y. <i>et al.</i> , "Experiments with HPS, A Restricted Data Flow Microarchitecture for High Performance Computers," <i>IEEE</i> , pp. 254-258 (1986).
	AQ	11	Patt, Y.N. <i>et al.</i> , "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," <i>IEEE</i> , pp. 75-81 (October 1986).
	AR	11	Swensen, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," <i>Conference Proceedings: 1988 International Conference on Supercomputing, ACM</i> , pp. 346-353 (July 4-8, 1988).

EXAMINER W. TREAT	DATE CONSIDERED 9/17/04
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				APPLICANT Deosaran <i>et al.</i>			
				FILING DATE February 27, 2002		GROUP 2172 2183	

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE	
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
	AJ12						
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	AL12						
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
WENT	AN	12	Uvieghara, G.A. <i>et al.</i> , "An Experimental Single-Chip Data Flow CPU," <i>Symposium on ULSI Circuits Design Digest of Technical Papers</i> , 2 pages (May 1990).
WENT	AO	12	Uvieghara, G.A. <i>et al.</i> , "An Experimental Single-Chip Data Flow CPU," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 27, No. 1, pp. 17-28 (January 1992).
WENT	AP	12	Wilson, J.E. <i>et al.</i> , "On Tuning the Microarchitecture of an HPS Implementation of the VAX," <i>Proceedings of the 20th Annual Workshop on Microprogramming</i> , IEEE Computer Society, pp. 162-167 (December 1-4, 1987).
	AQ	12	
	AR	12	

EXAMINER W. TRBAT	DATE CONSIDERED 9/17/04
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